

Appl. No. 10/622,863

Listing of Claims:

Claim 1(currently amended):

A method for manufacturing a nonvolatile memory on a substrate, said method comprising the steps of:

- forming a tunneling dielectric layer on said substrate;
- forming a first conductive layer on said tunneling dielectric layer;
- patterning said first polysilicon conductive layer, said tunneling dielectric layer and said substrate to form trenches therein;
- forming a gap-filling material into said trenches and over said substrate;
- removing a portion of said gap-filling material to form trench isolations and self-aligned first portion of a floating gate adjacent to said trench isolations;
- etching a portion of said trench isolations to form slots between said etched first conductive layer;
- forming a second conductive layer over a surface of said slots and said etched first conductive layer;
- etching said second conductive layer, thereby forming sidewall spacers on said slot;
- forming a second dielectric layer on said trench isolation, said sidewall spacers and said first conductive layer; and
- forming a third conductive layer on said second dielectric layer to act as a control gate.

Claim 2(original):

The method of claim 1, further comprising forming a fourth conductive layer before forming said second conductive layer.

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Claim 3(original):

The method of claim 1, wherein said tunneling dielectric layer comprises silicon oxide.

Claim 4(original):

The method of claim 1, wherein said second dielectric comprises ONO (oxide/nitride/oxide).

Claim 5(original):

The method of claim 1, wherein said second dielectric comprises ON (oxide/nitride).

Claim 6(original):

The method of claim 1, wherein said first conductive layer, second conductive layer, said third conductive layer are selected from polysilicon, alloy or metal.

Claim 7(currently amended):

A method for manufacturing a nonvolatile memory on a substrate, said method comprising the steps of:

- forming a tunneling dielectric layer on said substrate;
- forming a first conductive layer on said tunneling dielectric layer;
- patterning said first polysilicon conductive layer, said tunneling dielectric layer and said substrate to form trenches therein;
- forming a gap-filling material into said trenches and over said substrate;
- removing a portion of said gap-filling material to form trench isolations and self-aligned first portion of a floating gate adjacent to said trench isolations;

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etching a portion of said trench isolations to form slots between said etched first conductive layer;

forming a second dielectric layer on said trench isolation and said first conductive layer; and

forming a second conductive layer on said second dielectric layer to act as a control gate.

Claim 8(original):

The method of claim 7, further comprising forming a third conductive layer before forming said second dielectric layer; etching said third conductive layer to form sidewall spacers.

Claim 9(original):

The method of claim 7, wherein said tunneling dielectric layer comprises silicon oxide.

Claim 10(original):

The method of claim 7, wherein said second dielectric comprises ONO (oxide/nitride/oxide).

Claim 11(original):

The method of claim 7, wherein said second dielectric comprises ON (oxide/nitride).

Claim 12(original):

The method of claim 7, wherein said first conductive layer and said second conductive layer are selected from polysilicon, alloy or metal.